HT5581: USB-C PD 3.2 High-Power 240W Source/Sink Dual Role Port Controller

APPLICATIONS

- Power Bank
- Fast Charger Adaptor
- Consumer Electronics
- Laptop Computer
- 2 to 6 cells Lithium battery/lithium iron phosphate battery charging and discharging

GENERAL DESCRIPTION

HT5581 is an integrated battery charging and discharging DRP with Try.SRC protocol IC that supports charging and discharging power up to 240W. HT5581 supports various fast charging protocols such as PD3.2/ PD3.1 / PD3.0 / PD2.0 / QC3.0 / QC2.0 / BC1.2 / PPS and most DPDM fast charging protocols. HT5331 can be customized as PD Sink according to other power consumer applications.

HT5581 supports 2/3/4/5/6 serially connected battery cells. It also supports battery types of full charge voltage 3.65V / 4.1V / 4.2V / 4.35V / 4.4V.

HT5581 integrates a 11-bit ADC that enables IC temperature, battery NTC temperature.

HT5581 supports low-power standby mode. It will sleep automatically after an adjustable period of time in unattached state. A long press of an external tact switch connected to GPIO9 port will stop any discharging and enter low-power standby mode. Within in this mode, plugging in a charger can wake it up, a short press of the tact switch also perform the same function.

FEATURES

- 32-bit RISC-V microcontroller, Integrated Type-C USB compliant with PD3.2 Rev.1.0
- Source/Sink DRP with Try.SRC Protocol
- Maximum 240W power supply
- Type-C detect Sink / Source attached to activate discharge/charge circuit
- Up to 48V EPR FPDO, EPR AVS and PPS Supported
  - FPDO: 5V 3A, 9V 3A, 12V 3A, 15V 3A, 20V 5A EPR FPDO: 28V 5A, 36V 5A, 48V 5A
  - SPR AVS: 9V - 20V 5A
    EPR AVS: 15V - 48V 5A
    PPS: 5V – 21V 5A
- Multiple DPDM Charging Protocols Implemented
  - Apple 5V, 2.4A mode
  - BC1.2 DCP mode
  - QC2.0 5V/9V/12V and 20V
  - QC3.0 3.6V~20V continuous model voltage mode with 200mV step adjustment
- Sleep Mode
- EN Wake-up function
- Built-in VIN and VBUS pins fast discharge scheme
- Type-C Connector Pins Protection up to 50V
- Support cable drop compensation with 0, 50m, 100m/200mΩ selection
- Built-in adaptive UVP, adaptive OVP, I_OTP, CC_OVP and Fault Detections

DEVICE INFORMATION

Part Number	Package	Dimensions (mm)
HT5581	QFN24	4.0 x 4.0 x 0.75

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Typical Application Circuit

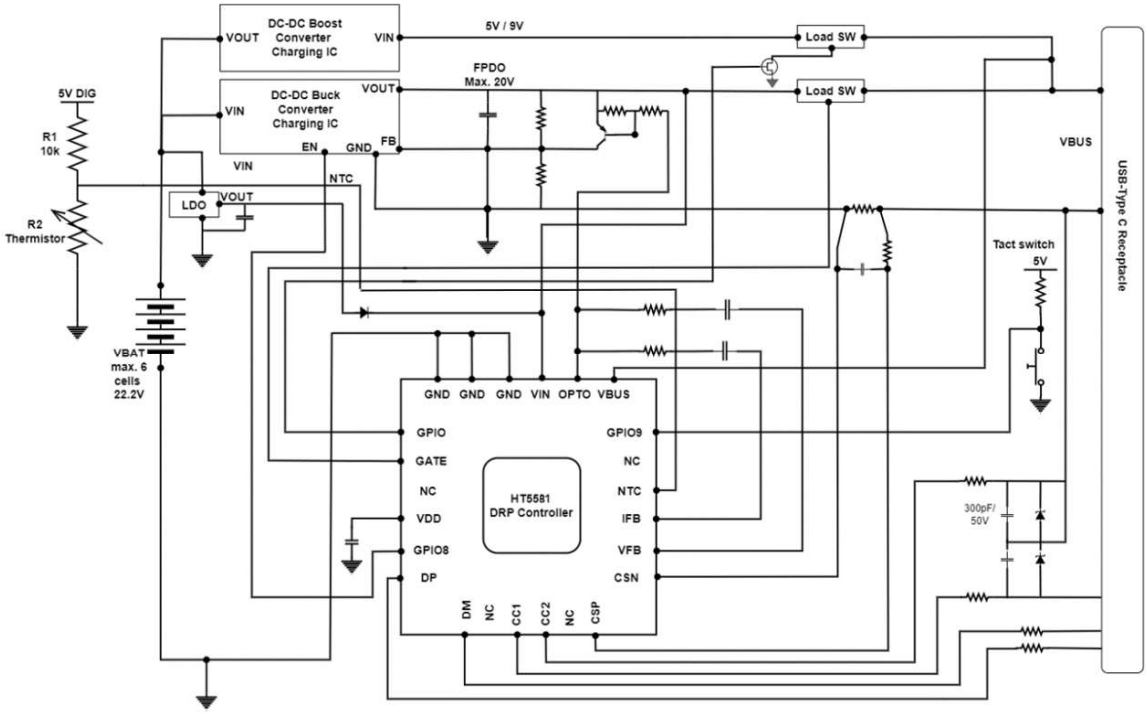

Figure 1 Typical Application Circuit of HT5581

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Behavioral and State Transition Diagram

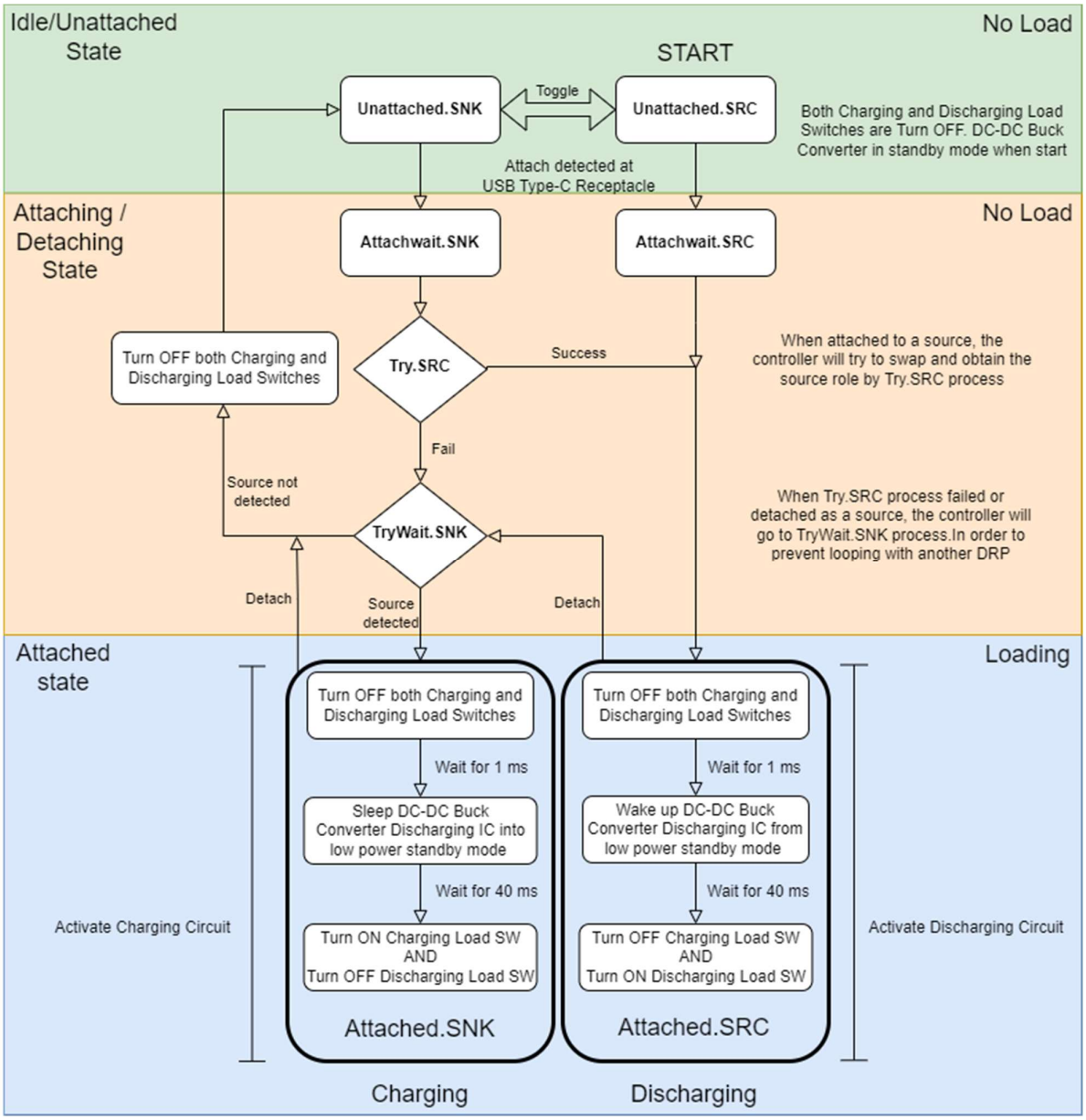

Figure 2.1 Charging / Discharging Operational Flow Chart

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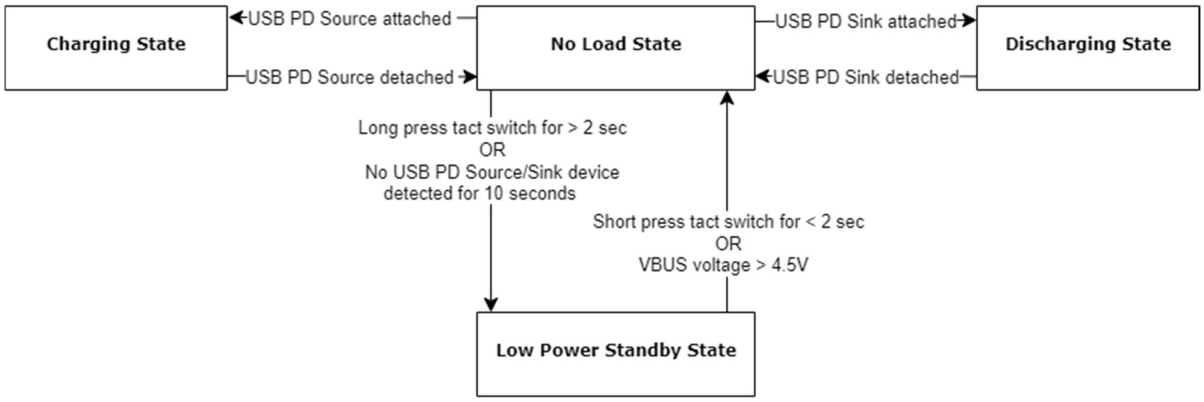

Figure 2.2 State Machine Diagram

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Pin Configuration

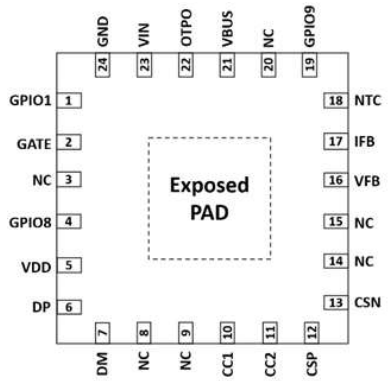

Figure 3. 24-pin DFN 4x4mm^2, TOP VIEW

Pin Functions

Pin No.	Pin Name	Pin Type	Voltage Type	Pin Description
1	GPIO1	Open Drain IO	LV	General purpose IO
2	GATE	Open Drain IO	HV	PMOS load switch gate driver.
3	NC	-	-	No Connection
4	GPIO8	Open Drain IO	LV	General purpose IO
5	VDD	Supply	LV	Internal 4.8V LDO output voltage. Connect this pin to GND via an 1uF ceramic capacitor.
6	DP	Analog IO	HV	USB D+ line
7	DM	Analog IO	HV	USB D- line
8	NC	-	-	No Connection
9	NC	-	-	No Connection
10	CC1	Analog IO	HV	USB Type-C Configuration Channel1
11	CC2	Analog IO	HV	USB Type-C Configuration Channel2
12	CSP	Analog I	LV	Positive input of the current sense amplifier.
13	CSN	Analog I	LV	Negative input of the current sense amplifier. Provide a low ohmic connection to GND.
14	NC	-	-	No Connection
15	NC	-	-	No Connection
16	VFB	Analog I	LV	Voltage loop feedback & compensation
17	IFB	Analog I	LV	Current loop feedback & compensation
18	NTC	Analog I	LV	NTC thermistor voltage sense
19	GPIO9	Open Drain IO	LV	General purpose IO
20	NC	-	-	No Connection
21	VBUS	Power	HV	VBUS sense and discharge sink
22	OPTO	Analog I	HV	Opto-coupler cathode pin on the secondary side provides feedback signal to the primary side PWM controller.
23	VIN	Power	HV	Supply input voltage. Connect this pin to GND via an 1uF ceramic capacitor.
24	GND	Power	-	Power ground

*Exposed pad is connected to GND if available

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