HT6329LV – High-Efficiency 36V Multiphase Dual-Buck DC-DC Controller for AI Processors (1V/100A, 2-/4-Phase Interleaved, Low-EMI)

APPLICATION

- Low-EMI Applications (Patented dithering technique)
- Automotive ADAS Power Supply
- CPU Power supply for NVIDIA/Qualcomm-like AI-Chipsets, in multi-phase operations
- USB Type C PD3.1 and Type A QC3.0 Fast Charging Application for dual-buck mode operations
- Automotive LED Lighting
- LCD / TV / Monitor Power

GENERAL DESCRIPTION

HT6329S is an easy to use, high efficiency, dual-channel outputs, synchronous step-down switching controller designed for high-power dual buck controller, in single chip.

HT6329S allows a wide input voltage range from 3.3V to 36V, and provides a wide range of output. It can also deliver up to 140W or higher with appropriate FETs at each channel. It also provides selectable switching frequency for circuit design with different size of inductor at high conversion efficiency and power density

HT6329S supports NVIDIA Open Voltage Regulator type-2, OpenVReg, with PWMVID feature to allow flexible adjustment of regulated output voltage from this PWM input controller

The external feedback provides the flexibility in interfacing with protocol IC to provide fast battery charging scheme like QC3.0 or PD3.1.

FEATURES

Dual-Channel Synchronous Buck Controller

- Wide input voltage range: 3.3V to 36V
- Wide output voltage regulated range: 1V to 24V
- Dual Channel with independent input voltage
- Dual channel or single-output multiphase
- Multiphase mode may have output up to 1V, 100A current in 4-phase operation by cascading of 2 devices.
- Support NVIDIA OpenVReg Type-2 with PWMVID application
- Selectable switching frequency at 300kHz, 500kHz and 700kHz
- Support Constant Current (CC) / Constant Voltage (CV) mode
- External Compensation

Multi-Protection

- Input under-voltage lockout (UVLO)
- Output over-voltage protection (OVP)
- Output short-circuits protection (SCP)
- Over-temperature protection (OTP)

DEVICE INFORMATION

Part Number	Package	Dimensions (mm)
HT6329LV	WQFN32	5.0 x 5.0 x 0.75

See package outline and dimension on page 12.

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Typical Application Circuit

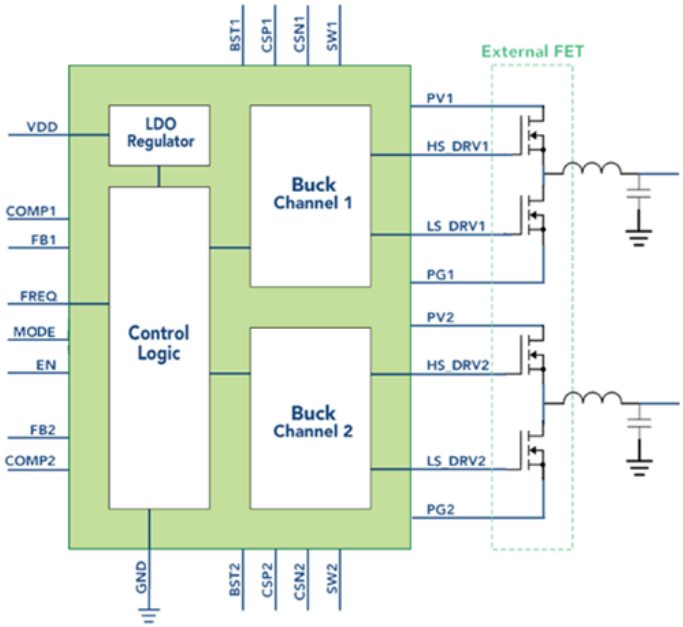

Fig. 1.1 – HT6329LV Dual-Outputs application Circuit

Conditions to operate at 2 Phases:

- **MODE pin >2.4V**, i.e tied it to **VDD**
- **COMP1 = COMP2** connected together
- **FREQ pin** as float, it will act as output pin, (default **FOSC=350K**)
- **FB2**, tied it to **GND**
- **Other pins** connected as usual

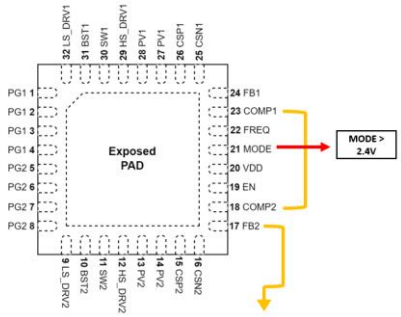

Fig. 1.2 – Detailed HT6329LV Application Circuit at Single-Output 2-Phases configuration

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Conditions to operate at 4 Phases:

- For master **DUT1**, set **MODE** pin = 5V
- For slave **DUT2**, set 0.8V < **MODE** < 2V, i.e. **MODE**=1V
- **COMP1** = **COMP2** = **COMP3** = **COMP4** connected together
- **FREQ_DUT1** pin as output **clk**
- **FREQ_DUT2** pin as input
- **FB1=FB3** connected, **FB2= FB4= GND**
- Other pins connected as usual

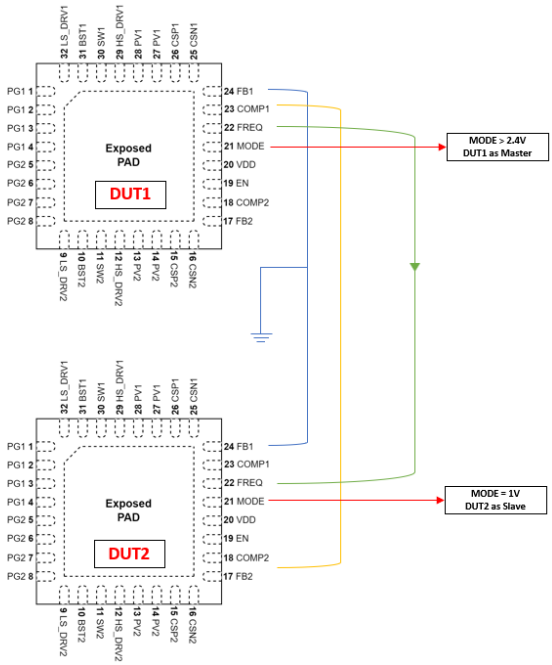

Fig. 1.3 – Detailed HT6329LV Application Circuit at Single-Output 4-Phases configuration

Pin Configuration

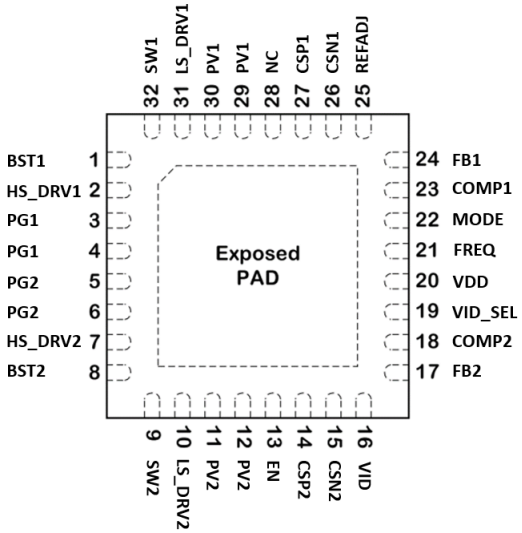

Fig. 2 - 32-pin WQFN, 5x5 mm^2, 0.5mm pitch TOP VIEW

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Pin Functions

Pin	Name	Description
1	BST1	Bootstrap Channel 1. Connect a capacitor and a resistor to SW1. Recommend 0.1uF and 2Ω.
2	HS_DRV1	High Side Gate Drive Channel 1
3,4	PG1	Power Ground Channel 1
5,6	PG2	Power Ground Channel 2
7	HS_DRV2	High Side Gate Drive Channel 2
8	BST2	Bootstrap Channel 2. Connect a capacitor and a resistor to SW2. Recommend 0.1uF and 2Ω.
9	SW2	Inductor Connection Channel 2
10	LS_DRV2	Low Side Gate Drive Channel 2
11,12	PV2	Input Power Channel 2. Connect a capacitor to GND. Recommend 1uF.
13	EN	Chip Enable. 1.35V enables the device. When V_{EN} > 8V, the device operates in forced PWM mode at light load and disables dithering.
14	CSP2	Current Sense Positive Channel 2
15	CSN2	Current Sense Negative Channel 2
16	VID	VID for OpenVReg, PWMVID input pin
17	FB2	Feedback Channel 2
18	COMP2	Compensation Channel 2
19	VID_SEL	Select pin for OpenVReg, active high for the usage of VID
20	VDD	VDD Regulator. Connect a decoupling capacitor to GND. Recommend 2.2uF.
21	FREQ	Frequency Selection Pin. See Application Information Section for detail.
22	MODE	Connect to GND for dual-output. Connect to VDD for interleaved single-output operation.
23	COMP1	Compensation Channel 1
24	FB1	Feedback Channel 1
25	REFADJ	Reference Adjustment. Connect this pin with a capacitor to have better reference (optional)
26	CSN1	Current Sense Negative Channel 1
27	CSP1	Current Sense Positive Channel 1
28	NC	
29, 30	PV1	Input Power Channel 1. Connect a capacitor to GND. Recommend 1uF.
31	LS_DRV1	Low Side Gate Drive Channel 1
32	SW1	Inductor Connection Channel 1
33	EPAD	Signal Ground & Thermal Dissipation Pad

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Absolute Maximum Ratings

PV1, PV2, SW1, SW2, EN	-0.3V to 40V
HS_DRV1, HS_DRV2, BST1, BST2	-0.3V to 36V
LS_DRV1, LS_DRV2	-0.3V to 6V
CSP1, CSN1, CSP2, CSN2	-0.3V to 22V
VDD, COMP1, COMP2, FB1, FB2, FREQ, MODE, PWM_IN, PWM_SEL, REFADJ	-0.3V to 6V
Operating Temperature Range	-40°C to 85°C
Maximum Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 125°C
Soldering Temperature	300°C

Electrical Characteristics (T_A=25°C, Vin = 12V unless specified)

Limits apply over the operating temperature range, unless else specified. Max and Min limits are provided through design, test or statistical dependence. Typical values are the most likely parametric norm at room temperature, and are stated for reference only. Unless otherwise specified the following conditions apply: VIN = 12V.

Parameters	Symbol	Test Conditions	Rating			Unit
			MIN	TYP	MAX	
Input Characteristics						
Input Voltage	V_{IN}		3.0		36	V
EN Threshold	V_{EN}			1.35		V
EN Hysteresis	V_{ENHYS}			110		mV
Quiescent Current	I_Q	Output at no load		1.5		mA
Shutdown Current	I_{stb}	V_{EN} = 0V		20		µA
Output Characteristics						
Output Voltage Range	V_{OUT}	V_{IN} = 36V	1.0		20	V
Output Current Limit	I_{Limit_FB}	R_{SENSE} = 10mΩ		3.6		A
Reference Voltage						
Output Voltage Reference	V_{FB}	Measured at FB1, FB2		1		V
Regulator Reference	V_{DD}	Measured at VDD		5.4		V
Switching Characteristics						
Switching Frequency	f_{sw}	FREQ=Z, MODE=0		300		kHz
		FREQ=L, MODE=0		500		kHz
		FREQ=H, MODE=0		700		kHz
		MODE > 1 V		350		KHz
Minimum On-Time	$t_{ON, Min}$			80		ns
Dither Generator						
Dither Modulation Frequency	f_{DITH}			1560		Hz
Maximum Switching Frequency	f_{OSCMAX}			850		kHz
Minimum Switching Frequency	f_{OSCMIN}			700		kHz
FREQ Pin (4-phase operation only)						
FREQ acts as output pin with 90 deg phase-shift clock		MODE=5V, device as master		300		KHz
FREQ acts as input pin to receive clock signal from master		MODE=1V, device as salve		3.5		V

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Parameters	Symbol	Test Conditions	Rating			Unit
			MIN	TYP	MAX	
MODE						
Mode input low threshold	V_{MODE_LOW}	Normal			0.6	V
Interleaved mode input high threshold as master	V_{MAS_HIGH}	2 / 4 phase multiphase	2.4			V
Interleaved mode input high threshold as slave	V_{SLV_HIGH}	4 phase multiphase	0.8		2	V
PWMVID Buffer and Selection						
VID_SEL input Low level	V_{VIDSEL_LOW}				0.6	V
VID_SEL input high level	V_{VIDSEL_HIGH}		1.2			V
VID_SEL input resistance	V_{VIDSEL_IR}			880		KΩ
VID input Low level	V_{VID_LOW}	PWMVID input			0.6	V
VID input high level	V_{VID_HIGH}	PWMVID input	1.2			V
VID input resistance	V_{VID_IR}			880		KΩ
REFADJ time constant	RC_{REFADJ}	Internal RC		20		MΩ
				5		pF
Gate Driver						
High-Side Gate driver Source	R_{HS_SRC}	I_{HS} = -50mA		4.5		Ω
High-Side Gate driver Sink	R_{HS_SNK}	I_{HS} = 50mA		1		Ω
Low-Side Gate driver Source	R_{LS_SRC}	I_{LS} = -50mA		4.5		Ω
Low-Side Gate driver Sink	R_{LS_SNK}	I_{LS} = 50mA		1		Ω
Dead Time	T_{DT}			25		ns
Input Under-voltage Lockout						
Input Under-Voltage Lockout Threshold High	V_{UVLO}			3.5		V
Input Under-Voltage Lockout Hysteresis	V_{UVHYS}		0.53	0.64	0.71	V
Output Under-voltage Lockout						
Output Under-voltage Protection	V_{UVP}			V_{OUT}*60%		V
Output Over-voltage Protection						
Output Over-Voltage Protection	V_{OVP}			V_{OUT}*130%		V
Over-Temperature Protection						
Thermal Shutdown	T_{SD}	Increasing Temperature		140		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}	Decreasing temperature		30		°C

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Functional Block Diagram

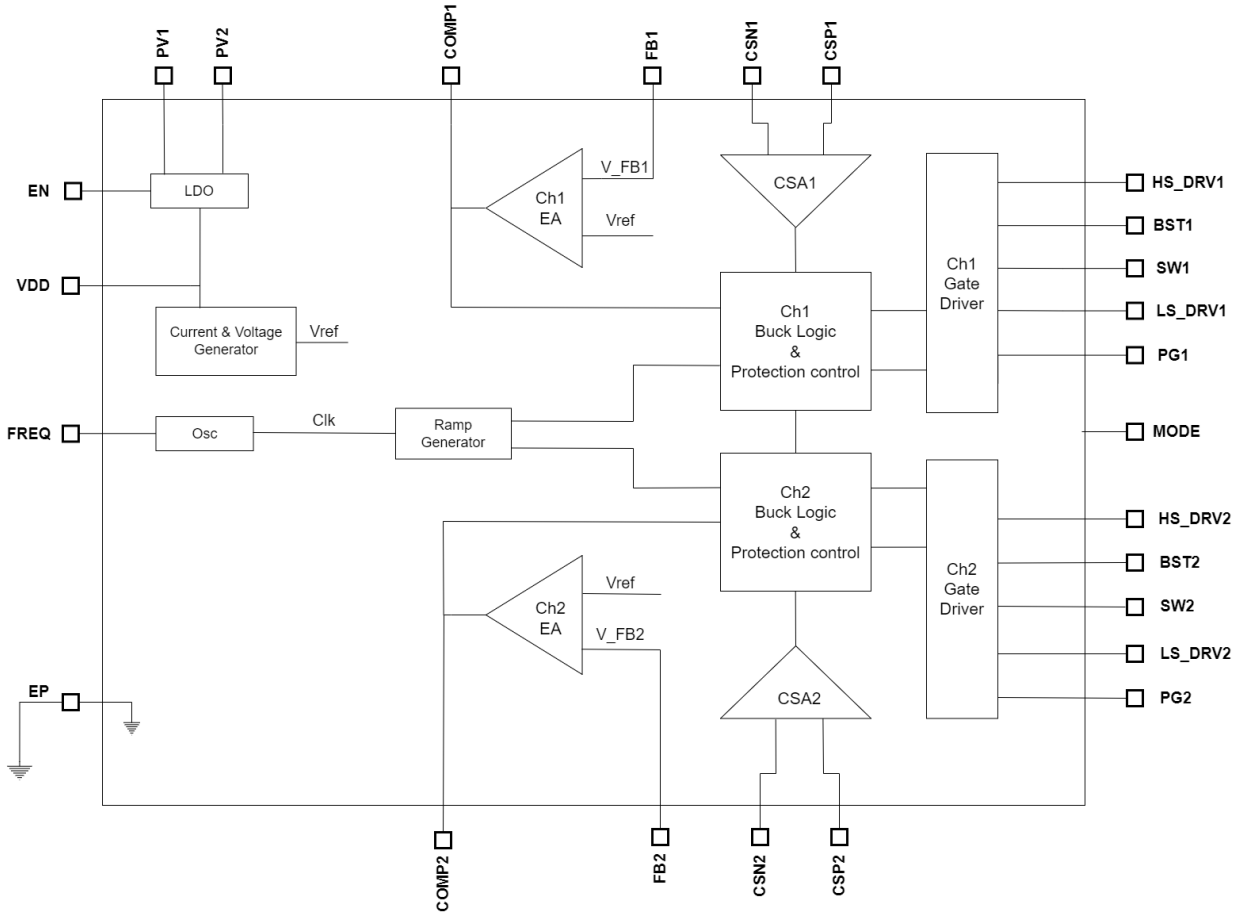

Fig. 3 – Functional Block Diagram

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Application Information

Input Protection

If the input voltage is smaller than Input UVLO, both buck channels stop the gate driver, reset and enter hiccup mode. It returns to Normal when the faults are cleared.

Output Protection

The Output Under-voltage Lockout threshold and the Output Over-voltage Protection are set at V_{OUT}*60% and V_{OUT}*130%. Once Output UVLO or OVP is triggered, the specific channel stops the gate driver, reset and enters hiccup mode.

Soft Start

HT6000 series employs an internal soft start in the buck converter to prevent large inrush current and overshoots of V_{OUT}. The soft start time is 20ms in the design.

Feedback and Output Voltage

HT6329LV provides an external FB for setting the output voltage. The feedback resistor divider tap is connected and V_{FB} is regulated at 1V. The relationship between the V_{OUT} and the resistor divider tap is as follows:

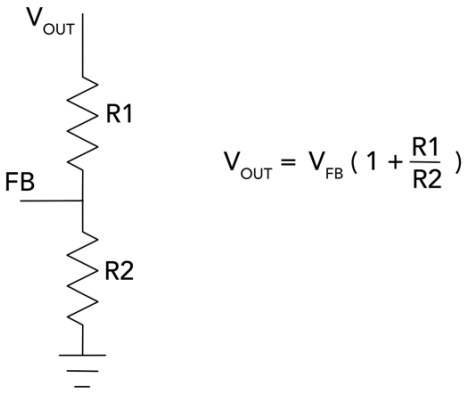

Fig. 4 – Feedback Resistor Network Design

Frequency Selection

At non-interleaved operation, the switching frequency can be selected by applying different conditions to the pin FREQ. As used as Single-Output multiphase operation (2-Phase/ 4-Phase), the switching frequency will be fixed at 350KHz operation.

FREQ state	f_{sw} (kHz)	**MODE (V)**
HZ (Floating)	300	0
L (Tied to GND)	500	0
H (Tied to VDD)	700	0
NA	350	>1

The efficiency of the conversion depends on the switching FET. Usually, the efficiency is higher at lower frequency because of lower switching loss.

Single-Output Multiphase operation by MODE levels selection

To configure a HT6329LV for multiphase operation (2/4-Phases), set Mode pin voltage higher than V_{MAS_HIGH}, e.g 2.4V to obtain the single-output multiphase operation. FREQ pin will be acted as clock output with 90° out of phase from the switching frequency for 4-Phase operation if needed. During in multiphase operation, switching frequency will be fixed at 350K Hz operation.

To configure for 4-Phases interleaved operation, two HT6329LV were used. One of device will act as master which its MODE pin > 2.2V and it will release the clock with 90° out of phase at FREQ pin. Another device will act as slave which its MODE pin > 1V but less than 2V, its FREQ pin will be used as input pin from master's synchronized clock to facilitate the 4-Phase interleaved operation.

MODE (V)	**Operation**	**Status**
0	Dual outputs	-
>2.4	2/4 Phases	Master
0.8< MODE <2	4 Phases	Slave

For the configurations for multiphases operations (2-Phases & 4-Phases) are shown as figure xxx & xxx

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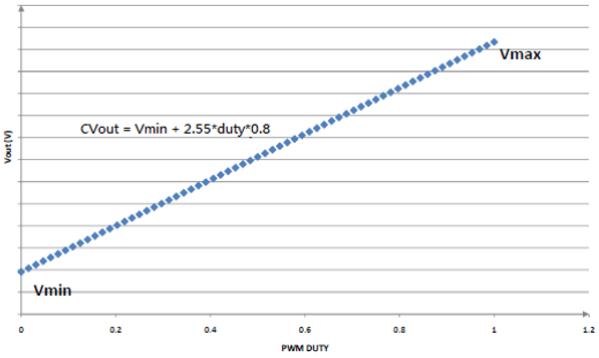
VID, VID_SEL & REFADJ for OpenVReg operation

The HT6329LV supports NVIDIA Open Voltage Regulator Type-2+ with PWMVID feature. By default, both VID & VID_SEL can be given as high impedance or "floated" so this feature is disabled. As VID_SEL > V_{VIDSEL_HIGH}, PWMVID input can be used and input will be buffered and filtered to generate the accurate reference voltage as the input of error amplifier for dc-dc regulation. The below figure is shown the relationship of the reference voltage, CVout, and the duty ratio of the PWMVID input.

CVout = Vmin*2.55*0.8*duty, where Vmin is 300mV.



The pin REFADJ as performance enhanced pin from the filtered PWMVID input signal, recommended 5pF ~ 10pF capacitor can be used at this pin to GND so to improve the ripple voltage of final output voltage of regulation.

Efficiency and External FET R_{dson}

The accuracy of the output voltage and the conversion efficiency is highly affected by the R_{dson} of the external FET. The lower the R_{dson} the higher the efficiency and voltage accuracy.

Compensation Network

The output of the Error Amplifier is connected to COMP pin, allowing external control loop compensation. A type-II compensation network is recommended to ensure system stability.

Constant Voltage / Constant Current Mode

HT6329S has the capability to operate in either CV (constant voltage) mode or CC (constant current) mode, with a smooth transition from CV to CC (See Fig.6). When in CV mode, it regulates the output voltage. Once the output current limit threshold is reached, HT6329S switches to CC mode. In CC mode, the output voltage decreases while the output current remains clamped at the predefined values. The current limit can be determined using the following equation.

$$I_{out(\max)} = \frac{36mV}{R_{sense}}$$

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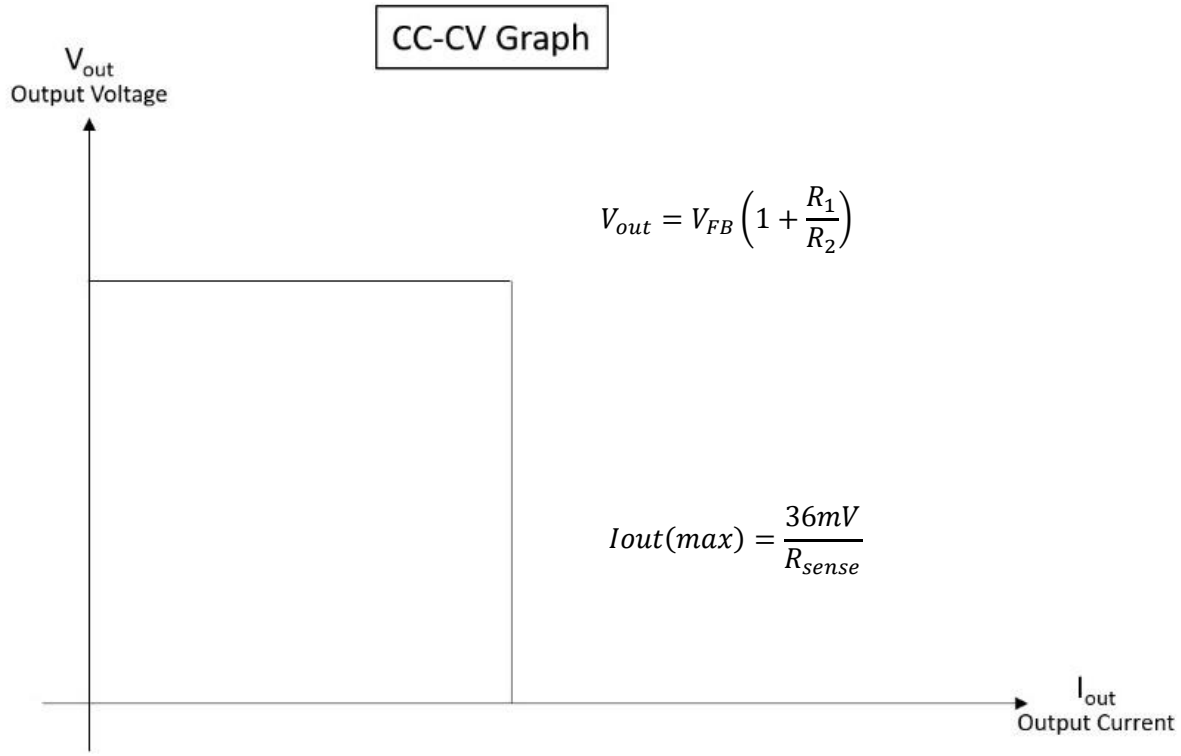

Fig. 5 - CC-CV Graph

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Typical Application Schematic

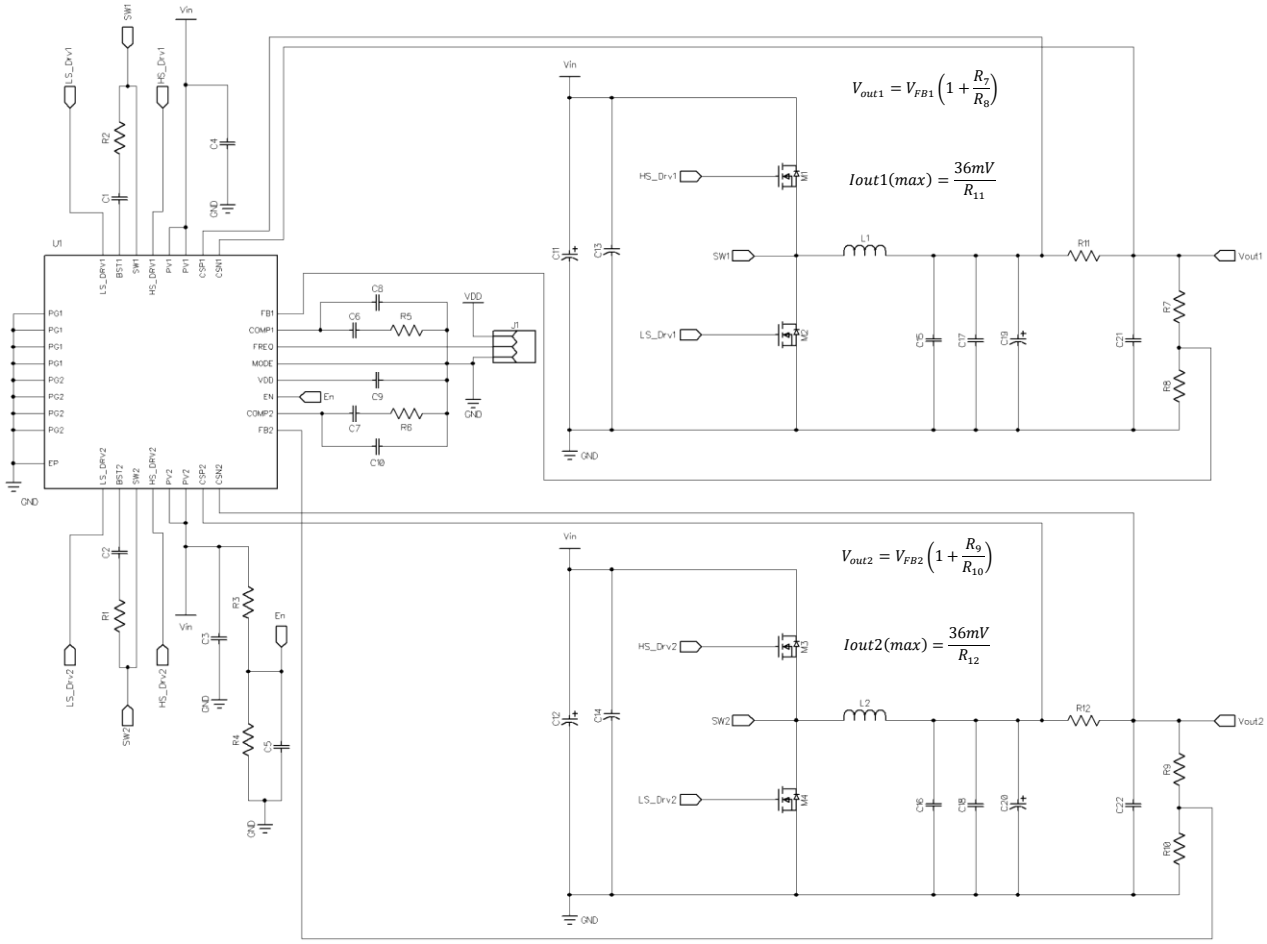

Fig. 6.1 - HT6329LV simplified schematic (MODE pin connects to GND)

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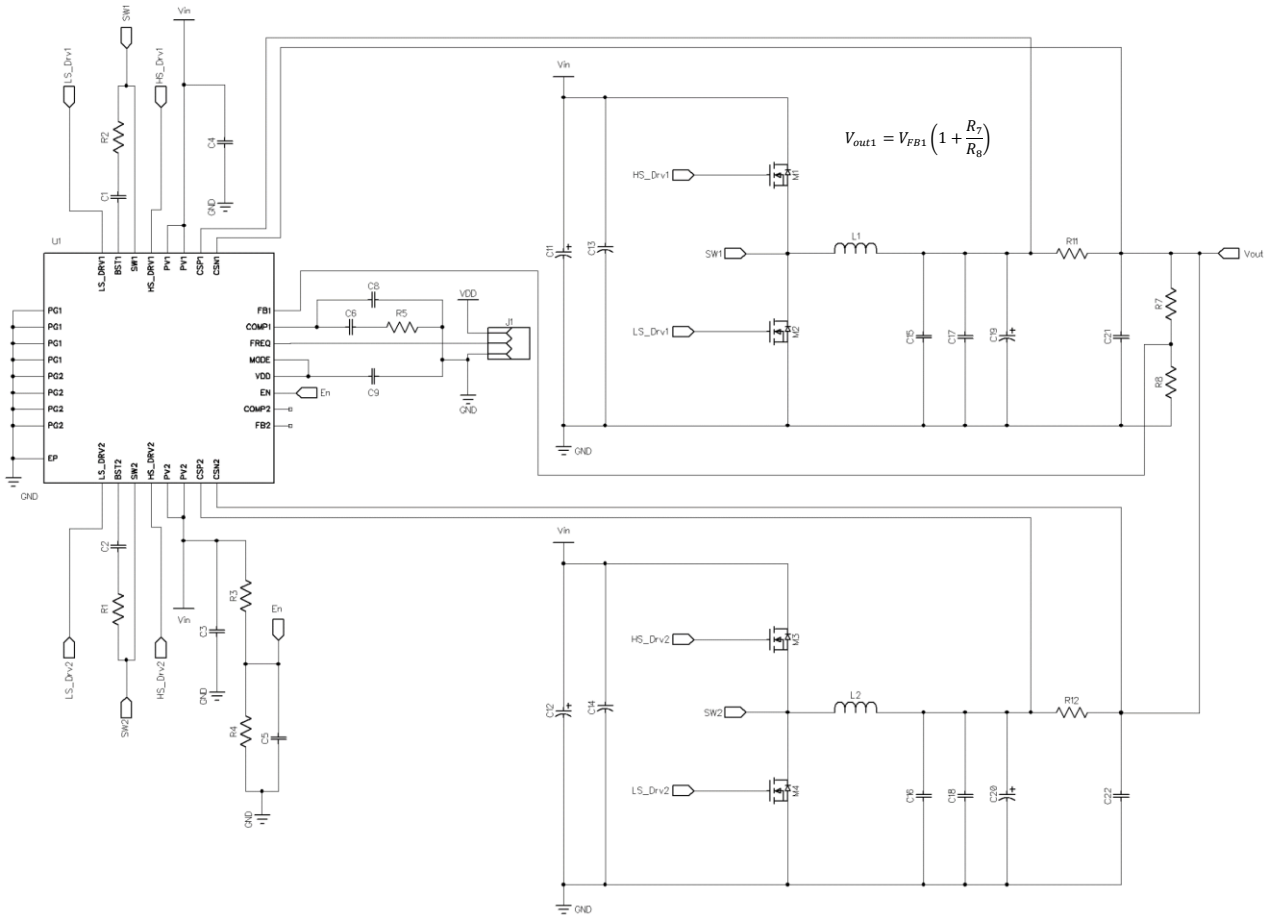

Fig. 6.2 - HT6329LV simplified schematic (MODE pin connects to VDD)

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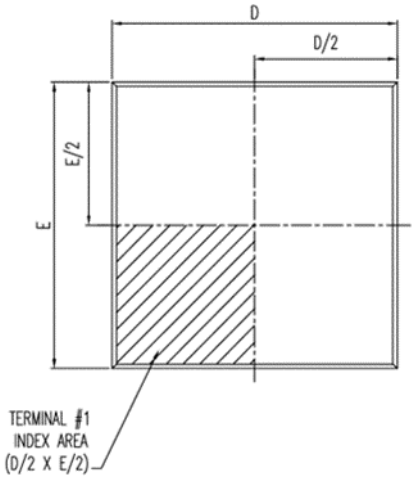
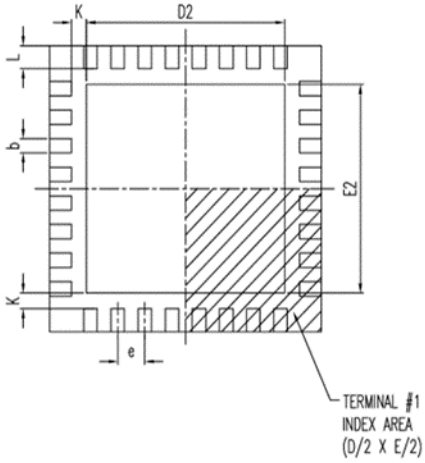
Package Outline and Dimensions

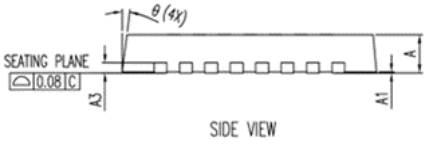
32-pin WQFN (5mm x 5mm, 0.5mm pitch)



Top View



Bottom View



Side View

SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF.	
D		5.00 BASIC	
D2	3.50	3.65	3.80
E		5.00 BASIC	
E2	3.50	3.65	3.80
e		0.50 BASIC	
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20		
θ	0°		14°
JEDEC	MO-220 (Variation WHHD-4)		

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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Dual Ports MAX SPEED

HT6000 Series

Fast Charging is just a Breeze

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